−300 mA, Ultralow Noise, High PSRR, Low Dropout Linear Regulator

Data Sheet **ADP7183**

FEATURES

- **Input voltage range: −2.0 V to −5.5 V**
- **Maximum output current: −300 mA**
- **Fixed output voltage options: −0.5 V to −4.5 V**
- **Adjustable output from −0.5 V to −V_{IN} + 0.5 V**
- **Low output noise: 4 μV rms from 100 Hz to 100 kHz**
- **Noise spectral density: 20 nV/√Hz, 10 kHz to 1 MHz**
- **Power supply rejection ratio (PSRR) at −300 mA load**
  - **75 dB typical at 10 kHz**
  - **62 dB typical at 100 kHz**
  - **40 dB typical at 1 MHz**
- **Low dropout voltage: −130 mV typical at I_{OUT} = −300 mA**
- **Initial output voltage accuracy (V_{OUT}): ±0.5% at I_{OUT} = −10 mA**
- **Output voltage accuracy over line, load, and temperature: ±2.6%**
- **Operating supply current (I_{GND}): −0.6 mA typical at no load**
- **Low shutdown current: −2 μA typical at V_{IN} = −5.5 V**
- **Stable with small 4.7 μF ceramic input and output capacitor**
- **Positive or negative enable logic**
- **Current-limit and thermal overload protection**
- **8-lead, 2 mm × 2 mm LFCSP package**
- **Supported by ADIsimPOWER voltage regulator design tool**

APPLICATIONS

- **Regulation to noise sensitive applications: analog-to-digital converters (ADCs), digital-to-analog converters (DACs), precision amplifiers**
- **Communications and infrastructure**
- **Medical and healthcare**
- **Industrial and instrumentation**

TYPICAL APPLICATION CIRCUITS

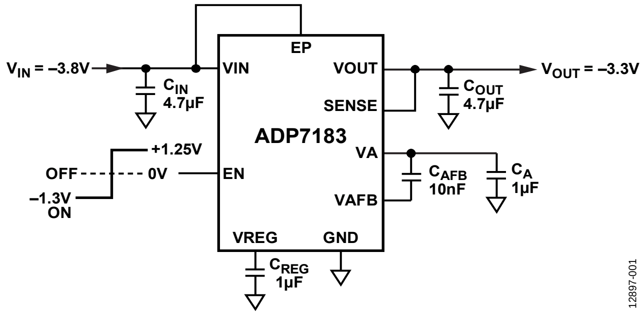

Figure 1. ADP7183 with Fixed Output Voltage, V_{OUT} = −3.3 V

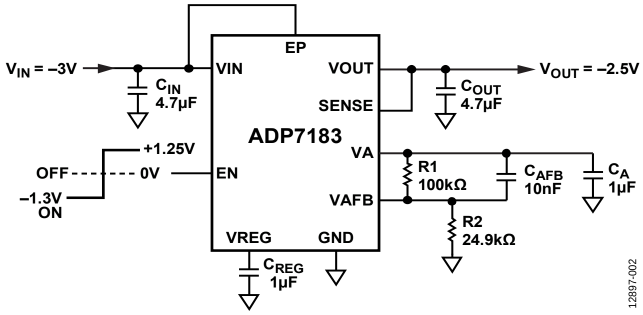

Figure 2. ADP7183 with Adjustable Output Voltage, V_{OUT} = −2.5 V

GENERAL DESCRIPTION

The ADP7183 is a complementary metal oxide semiconductor (CMOS), low dropout (LDO) linear regulator that operates from −2.0 V to −5.5 V and provides up to −300 mA of output current. This LDO regulator is ideal for regulation of high performance analog and mixed-signal circuits operating from −0.5 V down to −4.5 V. Using an advanced proprietary architecture, the ADP7183 provides high PSRR and low noise, and it achieves excellent line and load transient response with a small 4.7 μF ceramic output capacitor.

The ADP7183 is available in 15 fixed output voltage options. The following voltages are available from stock: −0.5 V, −1.0 V, −1.2 V, −1.5 V, −1.8 V, −2.0 V, −2.5 V, −3.0 V, and −3.3 V. Additional voltages available by special order are −0.8 V, −0.9 V, −1.3 V, −2.8 V, −4.2 V, and −4.5 V. An adjustable version is also available that allows output voltages that range from −0.5 V to −V_{IN} + 0.5 V with an external feedback divider.

The enable logic feature is capable of interfacing with positive or negative logic levels for maximum flexibility.

The ADP7183 regulator output noise is 4 μV rms independent of the output voltage. The ADP7183 is available in an 8-lead, 2 mm × 2 mm LFCSP, making it not only a very compact solution but also providing excellent thermal performance for applications requiring up to −300 mA of output current in a small, low profile footprint.

Rev. B **Document Feedback**

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5/2017—Rev. A to Rev. B

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2/2017—Rev. 0 to Rev. A

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10/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} − 0.5 V) or −2 V (whichever is more negative), EN = V_{IN}, I_{OUT} = −10 mA, C_{IN} = C_{OUT} = 4.7 µF, C_{AFB} = 10 nF, C_A = C_{REG} = 1 µF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		−2.0		−5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		−0.6	−0.90	mA
		I_{OUT} = −300 mA		−4.0	−7.0	mA
SHUTDOWN CURRENT	$I_{GND\text{-}SD}$	EN = GND, V_{IN} = −5.5 V		−2	−7	µA
OUTPUT NOISE[1]	OUT_{NOISE}	10 Hz to 100 kHz, C_{AFB} = 1 nF		7		µV rms
		10 Hz to 100 kHz, C_{AFB} = 10 nF		5		µV rms
		100 Hz to 100 kHz, C_{AFB} = 1 nF		6		µV rms
		100 Hz to 100 kHz, C_{AFB} = 10 nF		4		µV rms
NOISE SPECTRAL DENSITY[1]	OUT_{NSD}	100 Hz, C_{AFB} = 1 nF		300		nV/√Hz
		100 Hz, C_{AFB} = 10 nF		100		nV/√Hz
		10 kHz to 1 MHz, C_{AFB} = 1 nF to 1 µF		20		nV/√Hz
POWER SUPPLY REJECTION RATIO[1]	PSRR	I_{OUT} = −300 mA, V_{OUT} = −3.3 V, V_{IN} = −3.8 V				
		At 1 kHz		85		dB
		At 10 kHz		75		dB
		At 100 kHz		62		dB
		At 1 MHz		40		dB
OUTPUT VOLTAGE	V_{OUT}		−0.5		−4.5	V
Output Voltage Accuracy		I_{OUT} = −10 mA, T_A = 25°C	−0.5		+0.5	%
		−1 mA < I_{OUT} < −300 mA, V_{IN} = (V_{OUT} − 0.5 V) to −5.5 V	−2.6		+2.6	%
OUTPUT VOLTAGE REFERENCE FEEDBACK	V_{AFB}	Adjustable model voltage reference	−0.487	−0.5	−0.513	V
V_{AFB} Accuracy		Adjustable model, V_{IN} = −2 V, I_{OUT} = −10 mA	−2.6		+2.6	%
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} − 0.5 V) to −5.5 V	−0.1		+0.3	%/V
Load[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = −1 mA to −300 mA		0.8	2.6	%/A
INPUT BIAS CURRENT						
SENSE	$SENSE_{I\text{-}BIAS}$	−1 mA < I_{OUT} < −300 mA, V_{IN} = (V_{OUT} − 0.5 V) to −5.5 V		−10		nA
V_{AFB}	$V_{AFB\text{-}BIAS}$	−1 mA < I_{OUT} < −300 mA, V_{IN} = (V_{OUT} − 0.5 V) to −5.5 V		−10		nA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = −100 mA		−40	−65	mV
		I_{OUT} = −300 mA		−130	−220	mV
PULL-DOWN RESISTANCE		V_{EN} = 0 V				
Output Voltage	$V_{OUT\text{-}PULL}$	V_{OUT} = −1 V		280		Ω
Regulated Input Supply Voltage	$V_{REG\text{-}PULL}$	V_{REG} = −1 V		1.3		kΩ
Low Noise Reference Voltage	$V_{A\text{-}PULL}$	V_A = −1 V		61		Ω
START-UP TIME[4]	$t_{START\text{-}UP}$	V_{OUT} = −4.5 V, C_{AFB} = 1 nF, C_A = 1 µF		15		ms
		V_{OUT} = −4.5 V, C_{AFB} = 10 nF, C_A = 1 µF		55		ms
		V_{OUT} = −1.2 V, C_{AFB} = 1 nF, C_A = 1 µF		4		ms
		V_{OUT} = −1.2 V, C_{AFB} = 10 nF, C_A = 1 µF		10		ms
		V_{OUT} = −0.5 V, no C_{AFB}, C_A = 1 µF		1.5		ms
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}		−400	−600	−800	mA
THERMAL SHUTDOWN						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	$TS_{SD\text{-}HYS}$			15		°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UNDERVOLTAGE LOCKOUT THRESHOLDS						
Input Voltage						
Rising	$UVLO_{RISE}$				−1.77	V
Falling	$UVLO_{FALL}$		−1.58			V
Hysteresis	$UVLO_{HYS}$			90		mV
EN INPUT (NEGATIVE)		$-2\ V \leq V_{IN} \leq -5.5\ V$				
Logic High	$V_{EN\text{-}NEG\text{-}HIGH}$	V_{OUT} = off to on	−1.3	−1.16		V
Logic Low	$V_{EN\text{-}NEG\_LOW}$	V_{OUT} = on to off		−0.96	−0.88	V
Hysteresis	$EN_{HYS\text{-}NEG}$			191		mV
Leakage Current	$I_{EN\text{-}LKG}$	EN = V_{IN} or GND		−0.25		µA
EN INPUT (POSITIVE)		$-2\ V \leq V_{IN} \leq -5.5\ V$				
Logic High	$V_{EN\text{-}POS\text{-}HIGH}$	V_{OUT} = off to on		0.96	1.25	V
Logic Low	$V_{EN\text{-}POS\text{-}LOW}$	V_{OUT} = on to off	0.5	0.89		V
Leakage Current	$I_{EN\text{-}LKG}$	V_{EN} = 5 V, V_{IN} = −5.5 V		4.0	6.0	µA

[1] Guaranteed by characterization but not production tested.
[2] Based on an endpoint calculation using −1 mA and −300 mA loads.
[3] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages below −2 V.
[4] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current-limit threshold for a −3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of −3.0 V, or −2.7 V.

INPUT AND OUTPUT CAPACITOR RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE		T_A = −40°C to +125°C				
Minimum C_{IN} and C_{OUT} Capacitance[1]	C_{IN}, C_{OUT}		3.3	4.7		µF
Minimum C_A and C_{REG} Capacitance[2]	C_A, C_{REG}		0.7	1		µF
Minimum C_{AFB} Capacitance[3]	C_{AFB}		0.7	10		nF
Capacitor Equivalent Series Resistance (ESR)	R_{ESR}				0.1	Ω

[1] The minimum input and output capacitance must be greater than 3.3 µF over the full range of operating conditions. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.
[2] The minimum C_A and C_{REG} capacitance must be greater than 0.7 µF over the full range of operating conditions. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.
[3] The minimum C_{AFB} capacitance must be greater than 0.7 nF over the full range of operating conditions. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	+0.3 V to −6 V
VOUT to GND	+0.3 V to −V_{IN}
EN to GND	+5.0 V to −6 V
VA to GND	+0.3 V to −6 V
VAFB to GND	+0.3 V to −6 V
VREG to GND	+0.3 V to −2.16 V
SENSE to GND	+0.3 V to −6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7183 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}).

Use the following equation to calculate the junction temperature (T_J) from the ambient temperature (T_A) and power dissipation (P_D):

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction to ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction to ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The θ_{JA} value may vary, depending on the PCB material, layout, and environmental conditions. The specified θ_{JA} values are based on a 4-layer, 4 in. × 3 in. circuit board.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

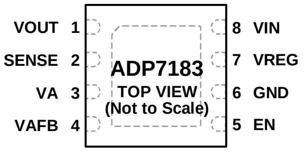
Package Type	θ_{JA}	θ_{JC}	Unit
CP-8-27[1]	68.8	10.0	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD ENHANCES THE THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO VIN INSIDE THE PACKAGE. IT IS RECOMMENDED THAT THE EXPOSED PAD CONNECT TO THE INPUT VOLTAGE PLANE ON THE BOARD.

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT	Regulated Output Voltage. Bypass the VOUT pin to the GND pin with a 4.7 µF or greater capacitor.
2	SENSE	Sense Input. Connect this pin to the VOUT pin.
3	VA	Low Noise Reference Voltage. Connect a 1 µF capacitor to GND to reduce noise. Do not connect a load to ground.
4	VAFB	Output Voltage Reference Feedback (Adjust Mode). Connect a 1 nF to 1 µF capacitor between the VAFB pin and the VA pin to reduce noise. Start-up time is increased as a function of the capacitance. Connect an external resistor divider between the VA pin and the VAFB pin to set the output voltage in adjust mode.
5	EN	Enable. Drive EN at least +1.25 V above or −1.3 V below ground to enable the regulator or drive EN to ground to turn the regulator off. For automatic startup, connect EN to VIN.
6	GND	Ground.
7	VREG	Regulated Input Supply to the LDO Amplifier. Bypass VREG to GND with a 1 µF or greater capacitor. Do not connect a load to ground.
8	VIN	Regulator Input Supply. Bypass VIN to GND with a 4.7 µF or greater capacitor.
	EP	Exposed Pad. The exposed pad enhances the thermal performance and is electrically connected to VIN inside the package. It is recommended that the exposed pad connect to the input voltage plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = -3.8$ V, $V_{OUT} = -3.3$ V, $I_{OUT} = -10$ mA, $C_{IN} = C_{OUT} = 4.7$ µF, $C_{AFB} = 10$ nF, $C_A = C_{REG} = 1$ µF, $T_A = 25$°C, unless otherwise noted.

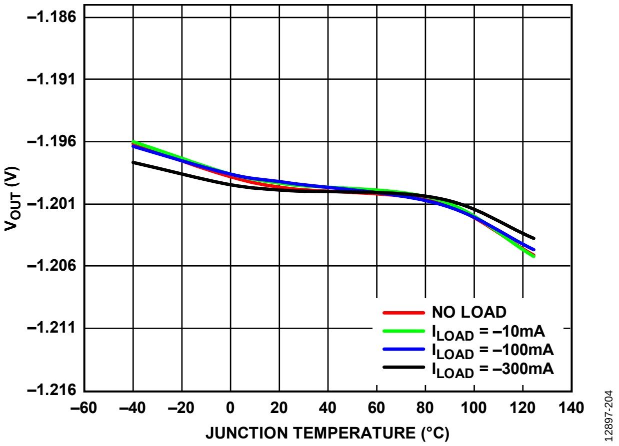


Figure 4. Output Voltage (V_{OUT}) vs. Junction Temperature, $V_{OUT} = -1.2$ V

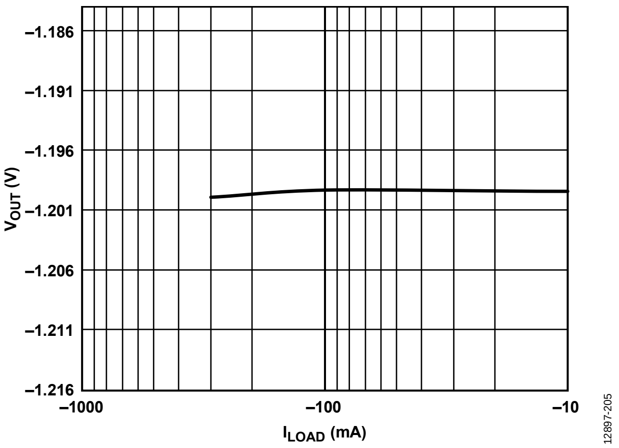


Figure 5. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), $V_{OUT} = -1.2$ V

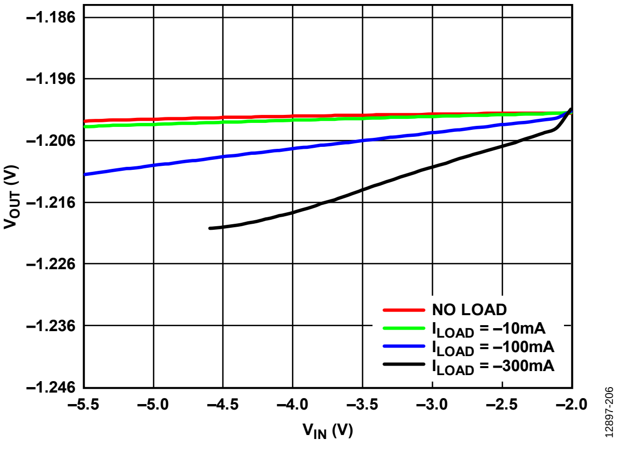


Figure 6. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), $V_{OUT} = -1.2$ V

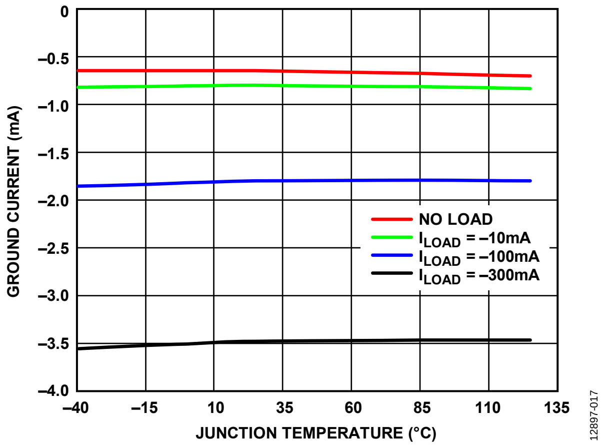


Figure 7. Ground Current vs. Junction Temperature (T_J), $V_{OUT} = -1.2$ V

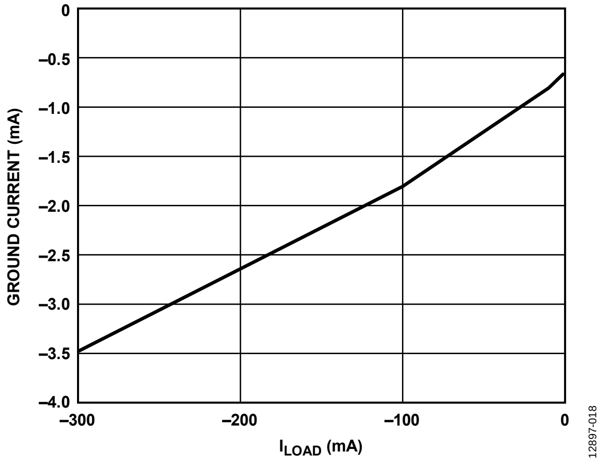


Figure 8. Ground Current vs. Load Current (I_{LOAD}), $V_{OUT} = -1.2$ V

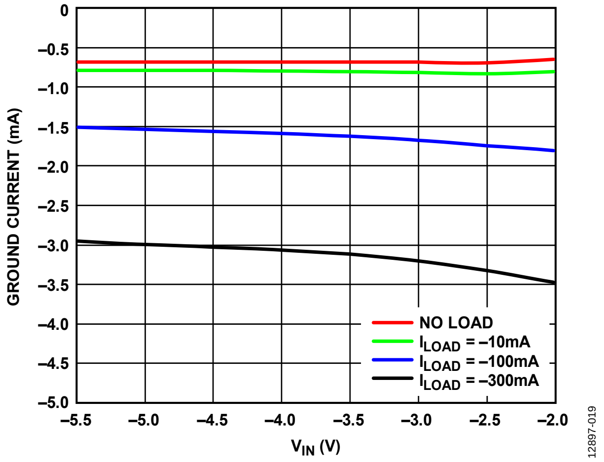


Figure 9. Ground Current vs. Input Voltage (V_{IN}), $V_{OUT} = -1.2$ V

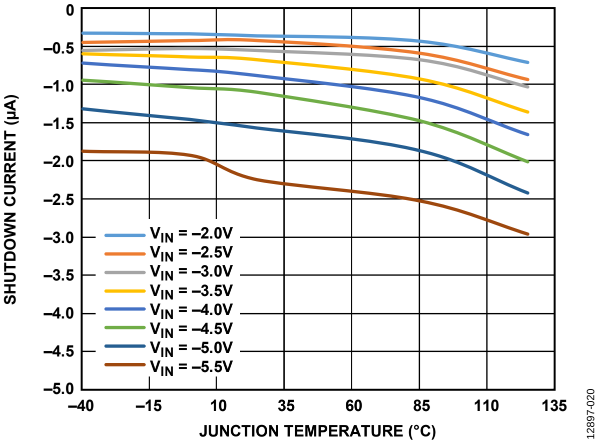


Figure 10. Shutdown Current vs. Junction Temperature at Various Input Voltages, V_{OUT} = −1.2 V

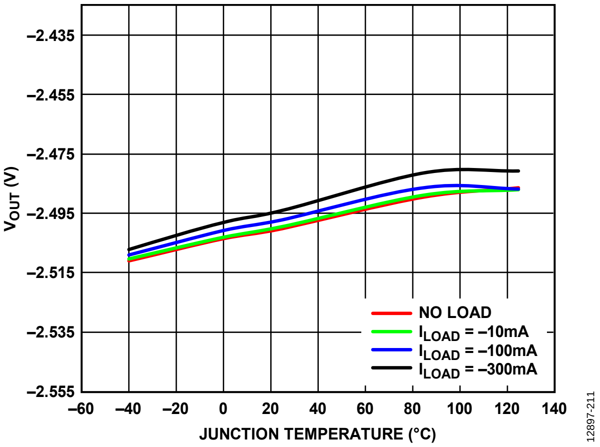


Figure 11. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = −2.5 V

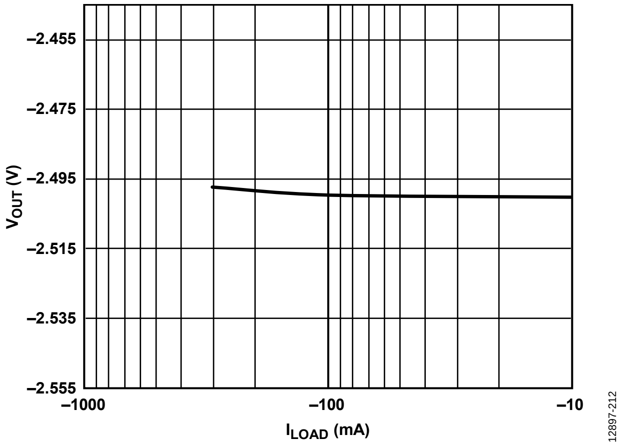


Figure 12. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = −2.5 V

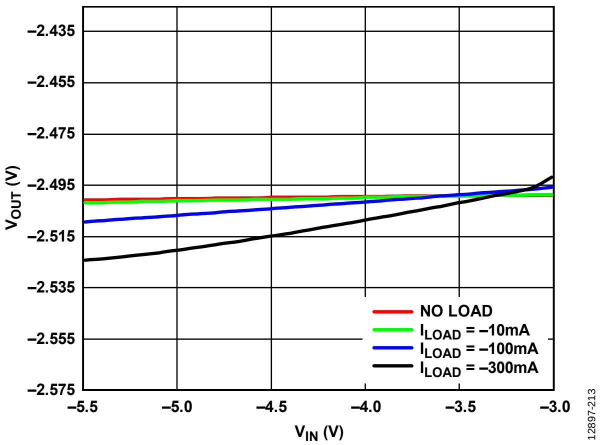


Figure 13. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = −2.5 V

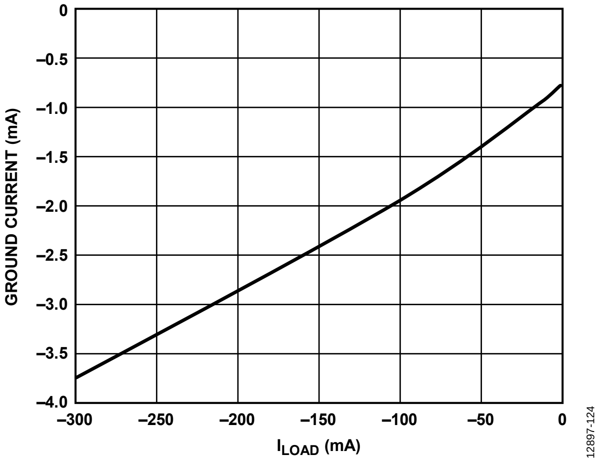


Figure 14. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = −2.5 V

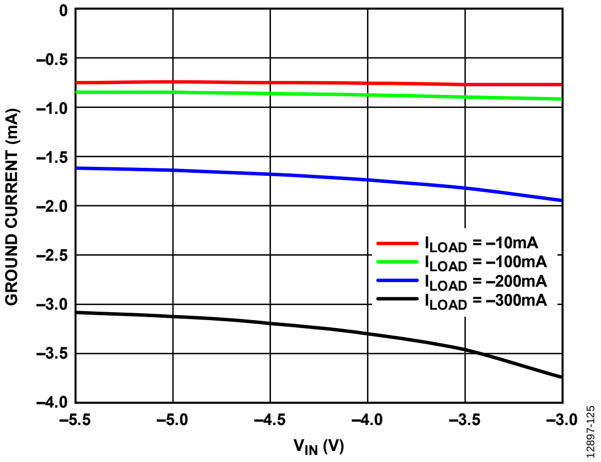


Figure 15. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = −2.5 V

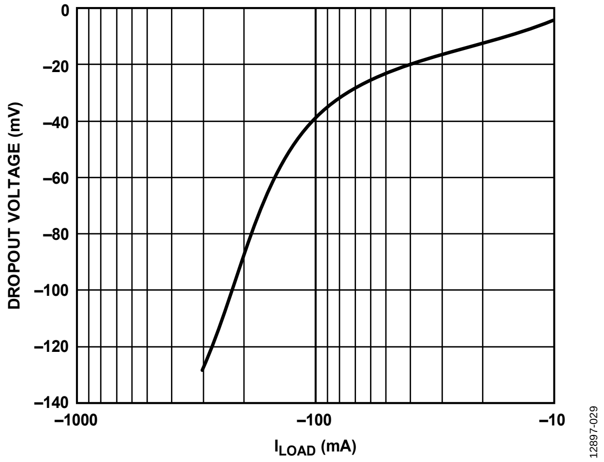


Figure 16. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = −2.5 V

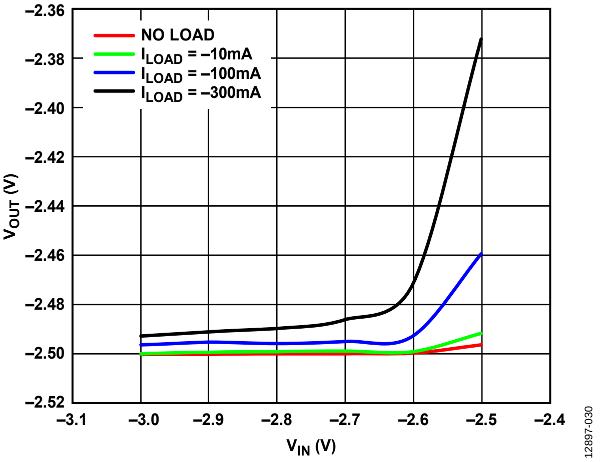


Figure 17. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout at Various Loads, V_{OUT} = −2.5 V

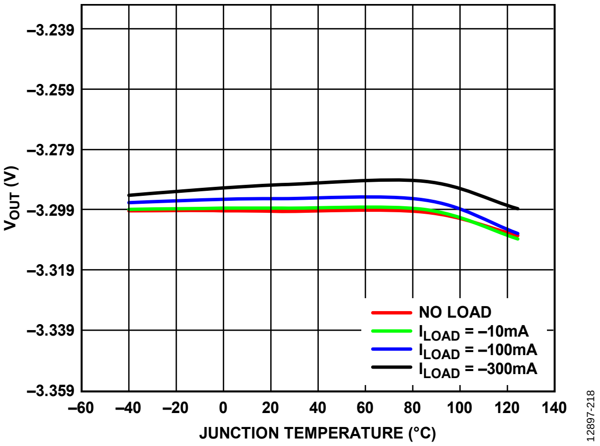


Figure 18. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = −3.3 V

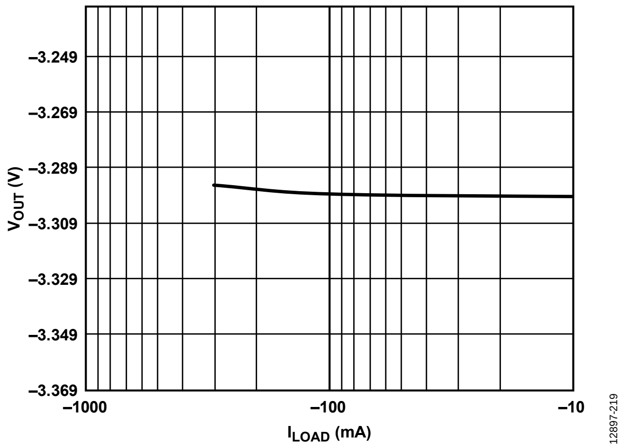


Figure 19. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = −3.3 V

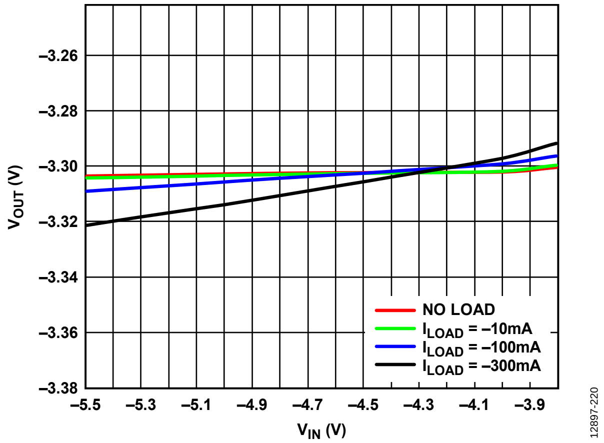


Figure 20. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = −3.3 V

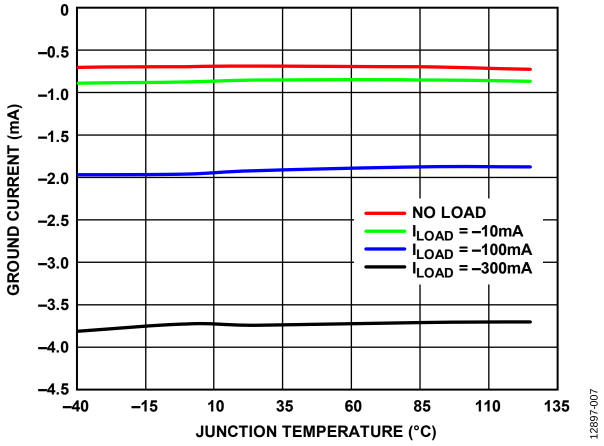


Figure 21. Ground Current vs. Junction Temperature (T_J), V_{OUT} = −3.3 V

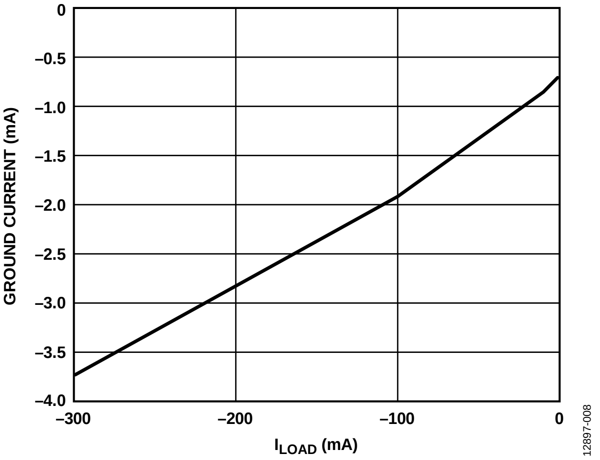


Figure 22. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = −3.3 V

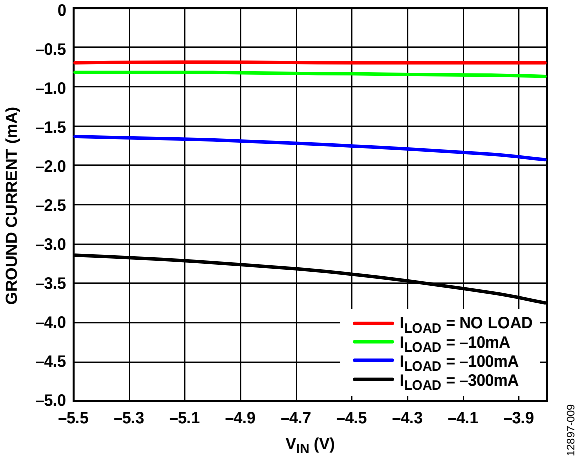


Figure 23. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = −3.3 V

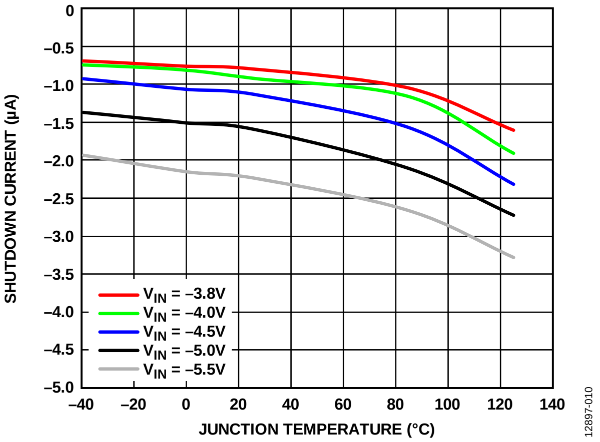


Figure 24. Shutdown Current vs. Junction Temperature (T_J) at Various Input Voltages, V_{OUT} = −3.3 V

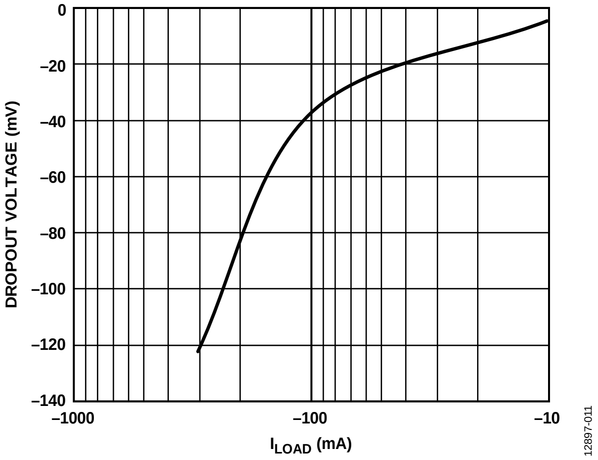


Figure 25. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = −3.3 V

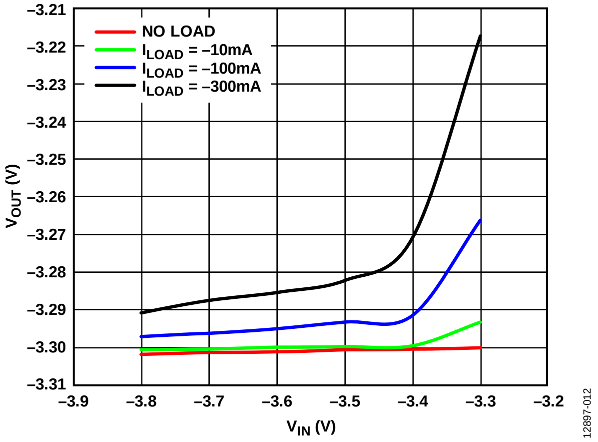


Figure 26. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout at Various Loads, V_{OUT} = −3.3 V

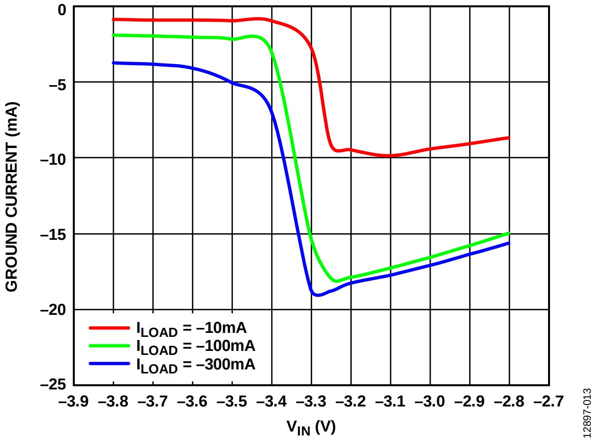


Figure 27. Ground Current vs. Input Voltage (V_{IN}) in Dropout at Various Loads, V_{OUT} = −3.3 V

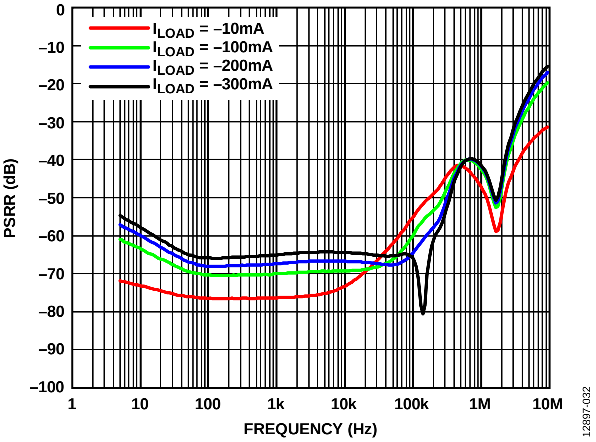


Figure 28. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = –1.2 V, V_{IN} = –2 V

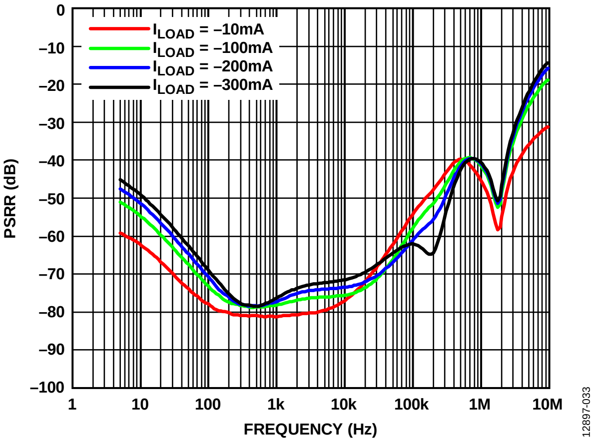


Figure 29. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = –2.5 V, V_{IN} = –3 V

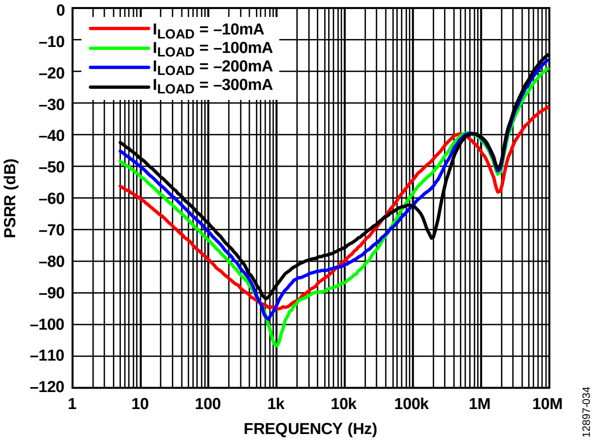


Figure 30. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = –3.3 V, V_{IN} = –3.8 V

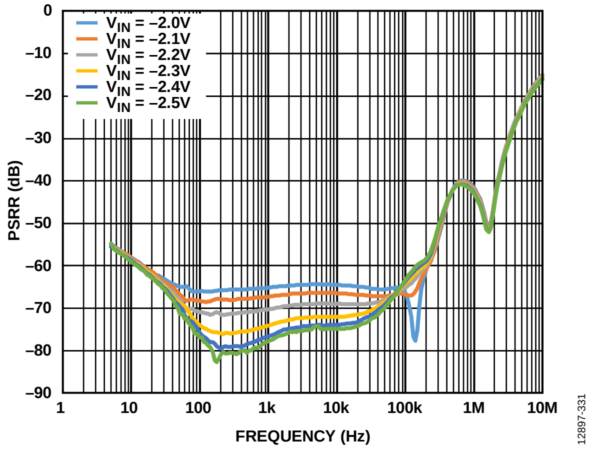


Figure 31. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Input Voltages, V_{OUT} = –1.2 V, I_{LOAD} = –300 mA

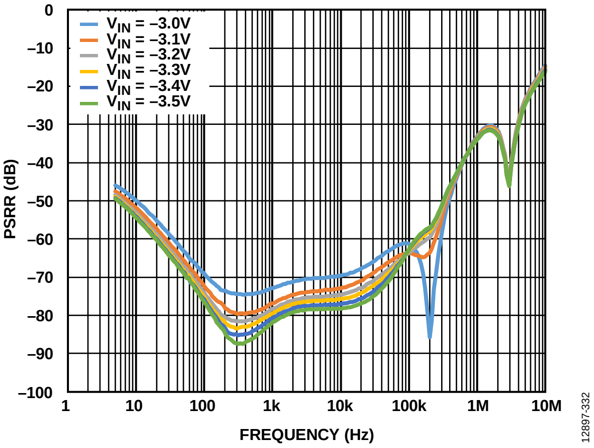


Figure 32. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Input Voltages, V_{OUT} = –2.5 V, I_{LOAD} = –300 mA

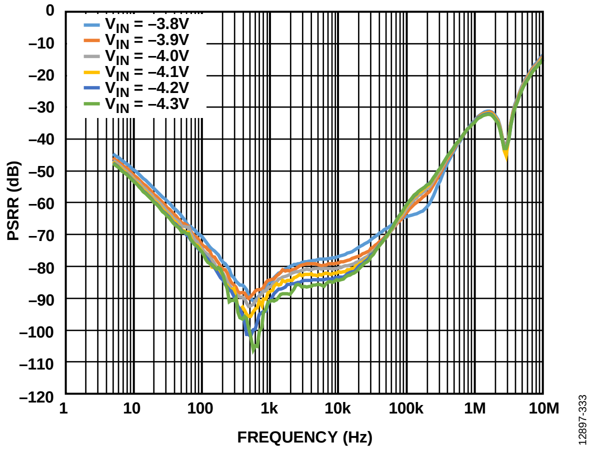


Figure 33. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Input Voltages, V_{OUT} = –3.3 V, I_{LOAD} = –300 mA

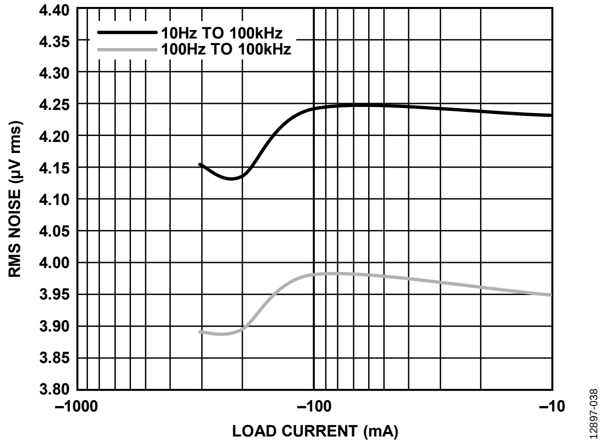


Figure 34. RMS Noise vs. Load Current (I_{LOAD}) at Various Frequencies

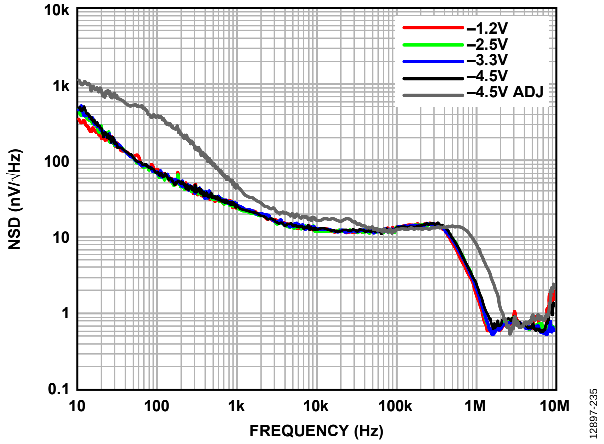


Figure 35. Noise Spectral Density (NSD) vs. Frequency at Various Output Voltages

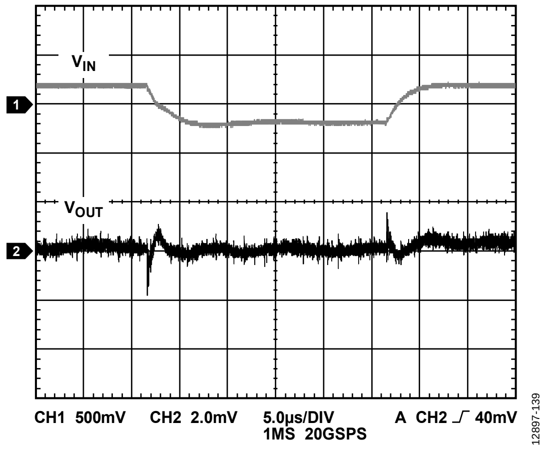


Figure 36. Line Transient Response, 500 mV Step, V_{OUT} = −1.2 V, I_{LOAD} = −300 mA

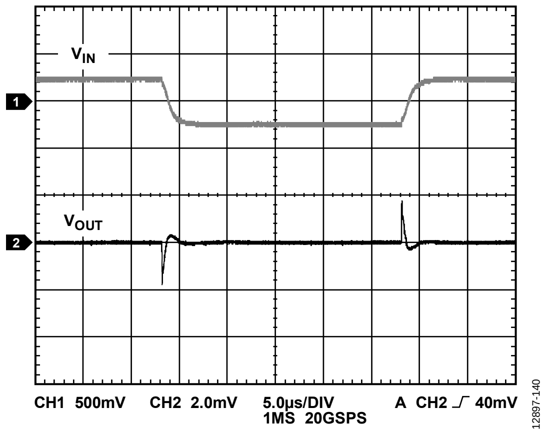


Figure 37. Line Transient Response, 500 mV Step, V_{OUT} = −3.3 V, I_{LOAD} = −300 mA

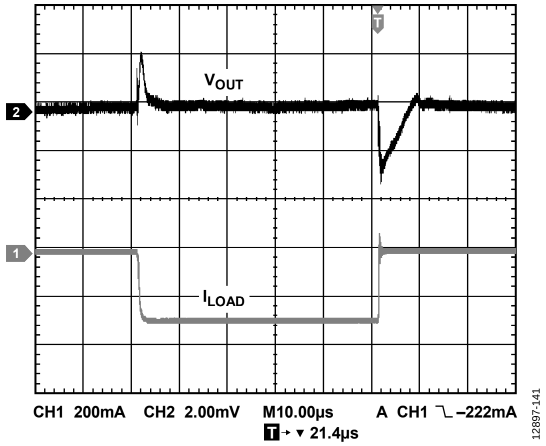


Figure 38. Load Transient Response, V_{OUT} = −1.2 V, I_{LOAD} = −10 mA to −300 mA

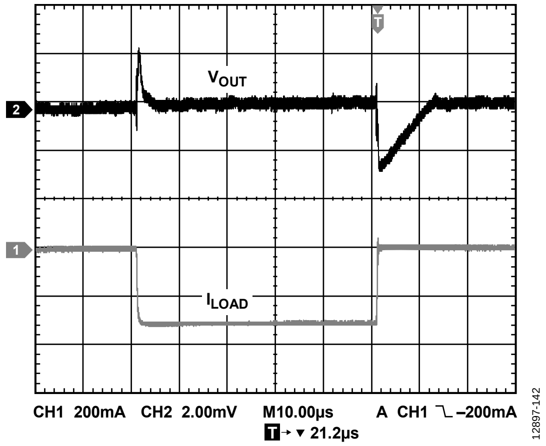


Figure 39. Load Transient Response, V_{OUT} = −2.5 V, I_{LOAD} = −10 mA to −300 mA

THEORY OF OPERATION

The ADP7183 is a low quiescent current, LDO linear regulator that operates from −2.0 V to −5.5 V and can provide up to −300 mA of output current. Total integrated output noise is 4 μV rms independent of the output voltage, making it ideal for high performance and noise sensitive applications. Shutdown current consumption is −7 μA (maximum).

The ADP7183 is optimized for use with a 4.7 μF ceramic capacitor for excellent transient performance. Using advanced proprietary architecture, the ADP7183 provides ultralow noise and high power supply rejection up to high frequencies of operation. Figure 40 shows the fixed output voltage internal block diagram of the ADP7183, and Figure 41 show the adjustable output voltage internal block diagram of the ADP7183.

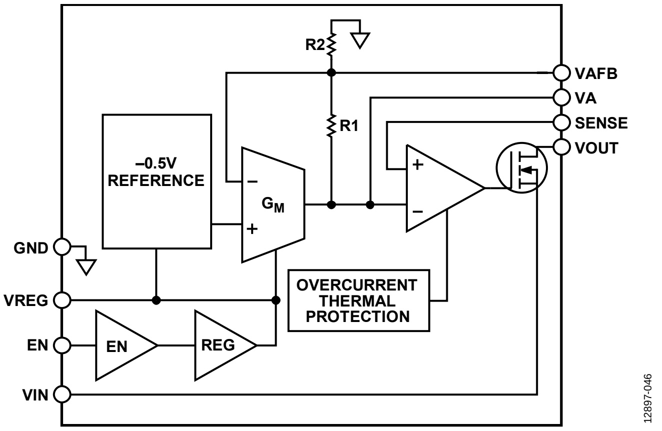


Figure 40. Fixed Output Voltage Internal Block Diagram

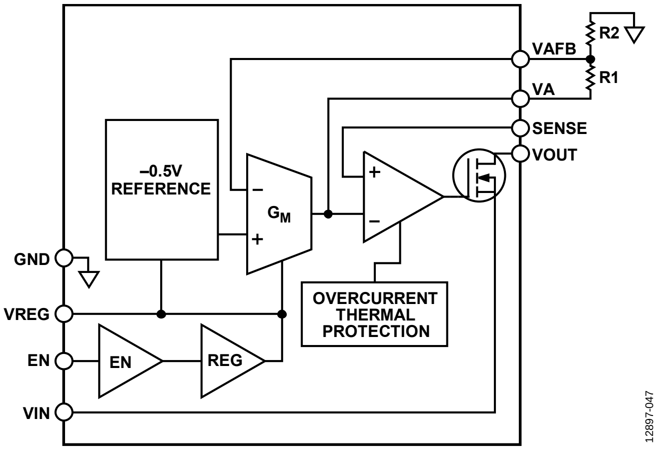


Figure 41. Adjustable Output Voltage Internal Block Diagram

Internally, the ADP7183 consists of a regulator block, reference block, G_M amplifier, feedback voltage divider, LDO regulator and a N channel MOSFET pass transistor. The regulator block produces an internal voltage rail (V_{REG}) of −1.8 V to serve as the supply voltage for the succeeding internal blocks. The G_M amplifier produces a reference voltage (V_A) used as a reference to the LDO regulator.

For fixed option models, the V_A voltage is generated through the resistor divider ratio depending on the V_{OUT} option. For adjustable models, the V_A voltage generates externally through the R1 and R2 resistors that are connected across the VA and VAFB pins. Because the reference voltage to the LDO regulator already adjusts according to the desired V_{OUT}, the LDO regulator now connects in a buffer configuration for improved noise performance. If the load draws higher current, the LDO regulator pulls the gate of the NMOS device higher towards GND to allow more current to pass. If the load draws less current, the LDO regulator pulls the gate of the NMOS device lower toward $-V_{IN}$ to restrict the amount of current passing through the device.

ADJUSTABLE MODE OPERATION

The adjustable mode version of the ADP7183 has an output that can be set to from −0.5 V to −4.5 V by an external voltage divider. To calculate the output voltage, use the following equation:

$$V_{OUT} = -0.5\ \text{V}(1 + R1/R2) \tag{1}$$

Figure 42 shows an example of an adjustable setting where R1 = 280 kΩ and R2 = 49.9 kΩ, setting the output voltage to −3.3 V.

R2 must be at least 10 kΩ to maximize PSRR performance.

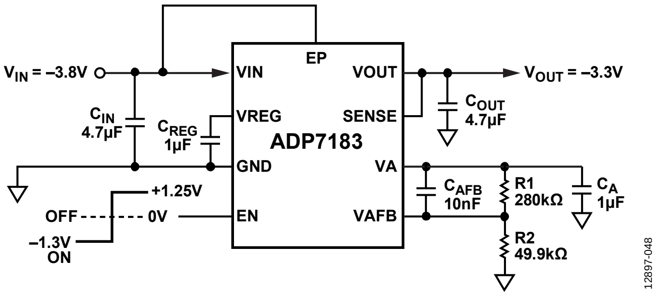


Figure 42. Setting the Adjustable Output Voltage

ENABLE PIN OPERATION

The ADP7183 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is +1.25 V above or −1.3 V below with respect to GND, VOUT turns on and when EN is at 0 V, VOUT turns off, as shown in Figure 43. For automatic startup, connect EN to VIN.

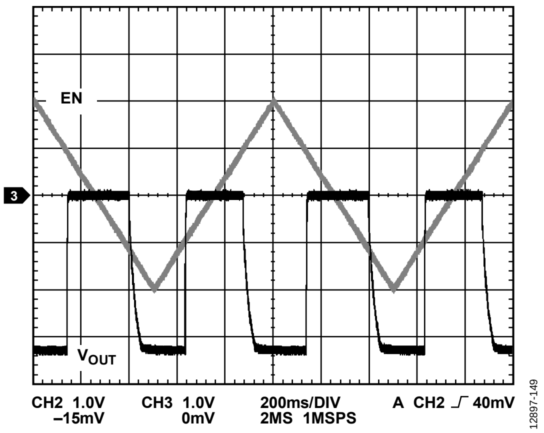


Figure 43. Typical EN Pin Operation

START-UP TIME

When the output is enabled, the ADP7183 uses an internal soft start to limit the inrush current. The start-up time for a −1.2 V output is approximately 12 ms from the time the EN active threshold is crossed to the time when the output reaches 90% of its final value (see Figure 44). As shown in Figure 44 and Figure 45, the start-up time is dependent upon the output voltage option and the value of the C_{AFB} capacitor.

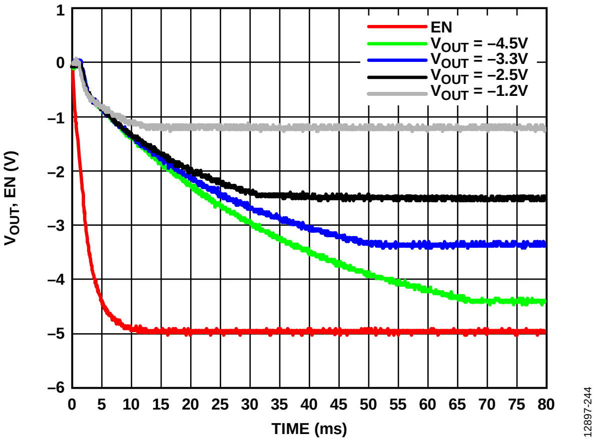


Figure 44. Start-Up Time at Various Output Voltages, C_{AFB} = 10 nF, C_A = 1 µF

The total start-up time depends mostly on the C_A and C_{AFB} values expressed by the τ_1 and τ_2 equations (see Equation 1 and Equation 2). During startup, an internal circuit, G_{M_START}, turns on and helps charge C_A up to 90% of the final value. Estimate the first time constant, τ_1, due to C_A by

$$\tau_1 \approx C_A \times ((R1 + R2)\ //\ Z_{OUT}) \tag{2}$$

During this time, keep Z_{OUT} low to approximately 1 kΩ to allow quick start-up times, keeping τ_1 in the order of 1 ms.

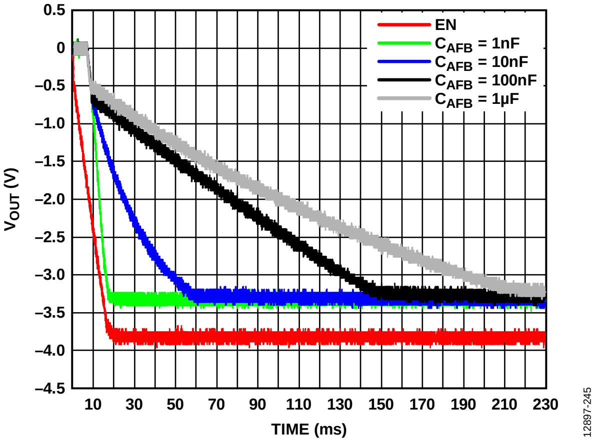


Figure 45. Start-Up Time at Various C_{AFB} Capacitor Values, C_A = 1 µF

A second time constant, τ_2, is dependent mainly on C_{AFB}. Figure 45 shows how the C_{AFB} value affects the start-up time. Estimate τ_2 by

$$\tau_2 \approx C_{AFB} \times R1 \tag{3}$$

The R1 value scales vs. the V_{OUT} option. Table 6 shows the R1 value depending on the fixed output voltage option, whereas R2 is constant at 500 kΩ. For example, at a fixed V_{OUT} = −3.3 V, R1 is equal to 2.8 MΩ. To keep τ_2 at a minimum, it is recommended that C_{AFB} be in the approximately nanofarad range. A typical setup for the ADP7183 is C_{AFB} = 10 nF; therefore, τ_2 = 28 ms. The total time constant, τ_{TOTAL}, is the sum of τ_1 and τ_2. At 2.2 × τ_{TOTAL}, VA is equal to ~90% of the final value. Therefore, for a fixed V_{OUT} = −3.3 V, the output voltage is ~90% of the final value after 63.8 ms.

Table 6. R1 and R2 Values for the Fixed Output Options

Output Voltage (V)	R1 (Ω)	R2 (kΩ)
−1.2	700 k	500
−2.5	2 M	500
−3.3	2.8 M	500
−4.5	4 M	500

Note that τ_1 and τ_2 are estimates only and do not take into account that G_M and Z_{OUT} dynamically change. It is an accurate estimate of ~90% of the start-up time for the C_{AFB} < 10 nF recommended setup, where ~100% of the settling time can easily be achieved. Note that for setups with C_{AFB} >> 10 nF, the equation may not hold true anymore. However, it is still a convenient estimate on the amount of time needed to achieve ~100% of the settling time.

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADIsimPower™ design tool set supports the ADP7183. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count, taking into consideration the operating conditions and limitations of the IC and all external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

CAPACITOR SELECTION

Output Capacitor

The ADP7183 operates with small, space-saving ceramic capacitors; however, it functions with general-purpose capacitors as long as care is taken with regard to the ESR value. The ESR of the output capacitor affects the stability of the LDO regulator control loop. A minimum of 4.7 µF capacitance with an ESR of 0.05 Ω or less is recommended to ensure the stability of the ADP7183. Output capacitance affects the transient response to changes in load currents. Using a larger value for the output capacitance improves the transient response of the ADP7183 to large changes in load current. Figure 46 shows the transient response for an output capacitance value of 4.7 µF.

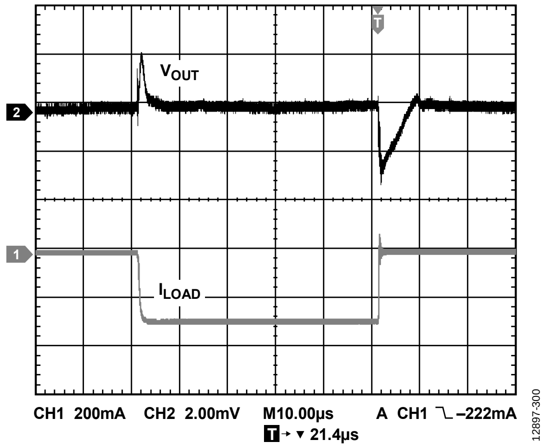


Figure 46. Output Transient Response, C_{OUT} = 4.7 µF, V_{OUT} = −1.2 V

Input Bypass Capacitor

Connecting a 4.7 µF or greater capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. When more than 4.7 µF of output capacitance is required, increase the input capacitance to match it.

C_A and C_{AFB} Capacitors

The ultralow output noise of the ADP7183 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. In this architecture, the resistor driven by the G_M amplifier adjusts the reference voltage to the selected output voltage. To ensure the G_M amplifier stability, the C_A capacitor is needed to generate the dominant pole and to keep the G_M amplifier stable across all conditions. C_A also serves as a dampening capacitor to the inputs of the LDO error amplifier for improved PSRR. However, the LDO output noise scales by the G_M amplifier amount of gain as a function of the output voltage. To minimize the output voltage noise contributed by the G_M amplifier, the C_{AFB} capacitor must be connected between the VA and VAFB pins to keep the ac gain of the G_M amplifier in unity.

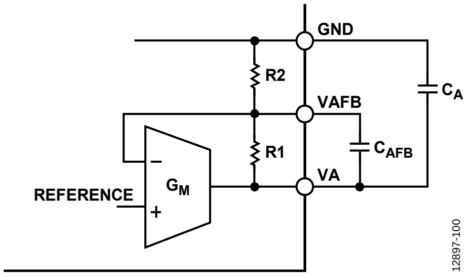


Figure 47. C_A and C_{AFB} Connection to G_M Amplifier

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP7183 if they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R and X7R dielectrics with a voltage rating from 6.3 V to 10 V are recommended. Due to their poor temperature and dc bias characteristics, Y5V and Z5U dielectrics are not recommended.

Figure 48 shows the capacitance change vs. the bias voltage characteristics of a 0805 case, 4.7 µF, 10 V, X5R capacitor. The capacitor size and voltage rating strongly influences the voltage stability of a capacitor. In general, a capacitor in a larger package or with a higher voltage rating exhibits improved stability. The temperature variation of the X5R dielectric is about ±15% over the −55°C to +85°C temperature range and is not a function of package size or voltage rating.

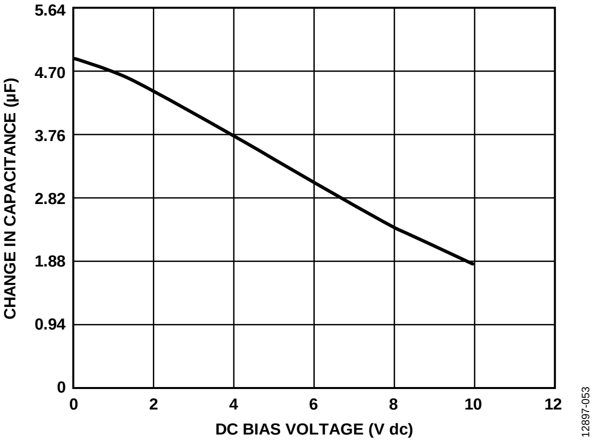


Figure 48. Change in Capacitance vs. DC Bias Voltage

Use Equation 4 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - Tempco) \times (1 - TOL) \tag{4}$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
C_{OUT} is the output capacitor.
Tempco is the worst case capacitor temperature coefficient.
TOL is the worst case component tolerance.

In this example, the worst-case temperature coefficient (Tempco) over −55°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} = 4.7 µF at 1.0 V.

Substituting these values in Equation 4 yields

$$C_{EFF} = 4.7\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.6\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO regulator over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP7183, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT (UVLO)

The UVLO circuitry protects the system from power supply brownouts. If the input voltage on VIN is more positive than the minimum −1.58 V UVLO falling threshold, the LDO output shuts down. The LDO enables again when the voltage to VIN is more negative than the maximum −1.77 V UVLO rising threshold.

A typical hysteresis of 90 mV within the UVLO circuitry prevents the device from oscillating due to the noise from VIN.

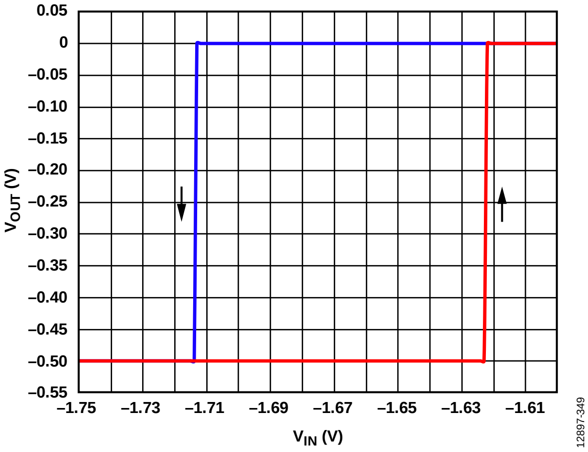


Figure 49. Typical UVLO Behavior, V_{OUT} = −0.5 V

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP7183 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP7183 is designed to reach the current limit when the output load reaches −600 mA (typical). When the output load exceeds −600 mA, the output voltage reduces to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a threshold of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature begins to rise above 150°C, the output turns off, reducing the output current to zero. When the junction temperature drops below 135°C (typical), the output turns on again, and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP7183 reaches the current limit so that only −600 mA is conducted into the short. If self heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to 0 mA. As the junction temperature cools and drops below 135°C, the output turns on and conducts −600 mA into the short circuit, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between −600 mA and 0 mA that continues as long as the short remains at the output. Current-limit and thermal overload protections protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with a low input-to-output voltage differential, the ADP7183 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough to cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. The converter recovers only after the junction temperature decreases below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 5.

To guarantee reliable operation, the junction temperature of the ADP7183 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used, and the amount of copper used to solder the package VIN pins to the PCB.

Table 7 shows the typical θ_{JA} values for the 8-lead LFCSP package for various PCB copper sizes.

Table 7. Typical θ_{JA} Values for the 8-Lead LFCSP

Copper Size (mm²)	θ_{JA} (°C/W)
25	146.6
100	105.4
500	75.38
1000	65.16
6400	53.5

Calculate the junction temperatures of the ADP7183 by

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (5)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{OUT}) \times I_{LOAD}) + (V_{IN} \times I_{GND}) \quad (6)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_A + (((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \theta_{JA}) \quad (7)$$

As shown in Equation 7, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C.

Figure 50 to Figure 52 show the junction temperature calculations for the different ambient temperatures, power dissipation, and areas of the PCB copper.

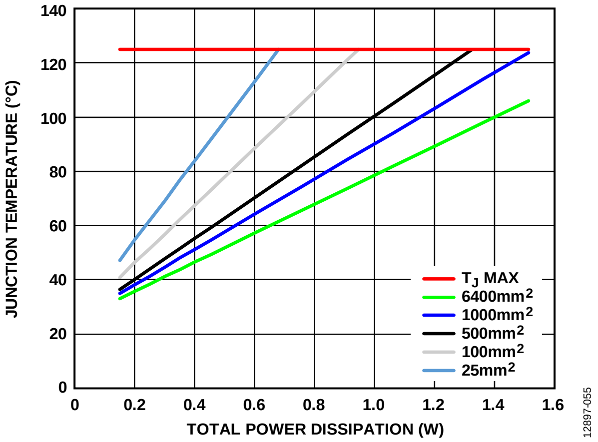


Figure 50. Junction Temperature vs. Total Power Dissipation, T_A = 25°C

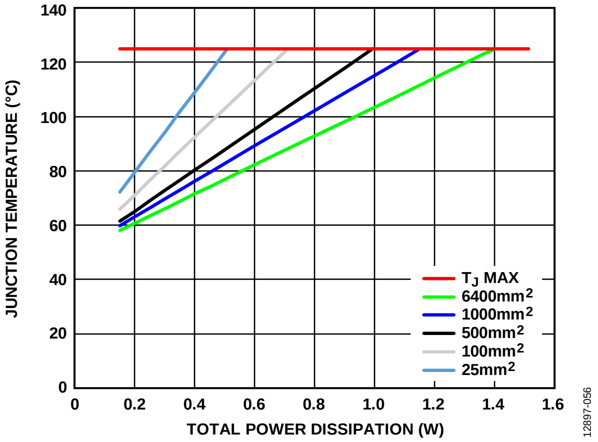


Figure 51. Junction Temperature vs. Total Power Dissipation, T_A = 50°C

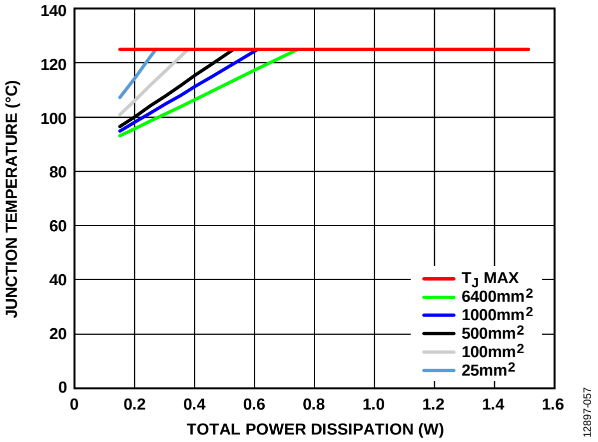


Figure 52. Junction Temperature vs. Total Power Dissipation, T_A = 85°C

PCB LAYOUT CONSIDERATIONS

Place the input capacitor (C_{IN}) as close as possible to the VIN and GND pins. Place the output capacitor (C_{OUT}) as close as possible to the VOUT and GND pins. Place bypass capacitors (C_A and C_{REG}) close to the respective pins (VA and VREG) and GND. Use of 0805 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited. Connect the exposed pad to VIN.

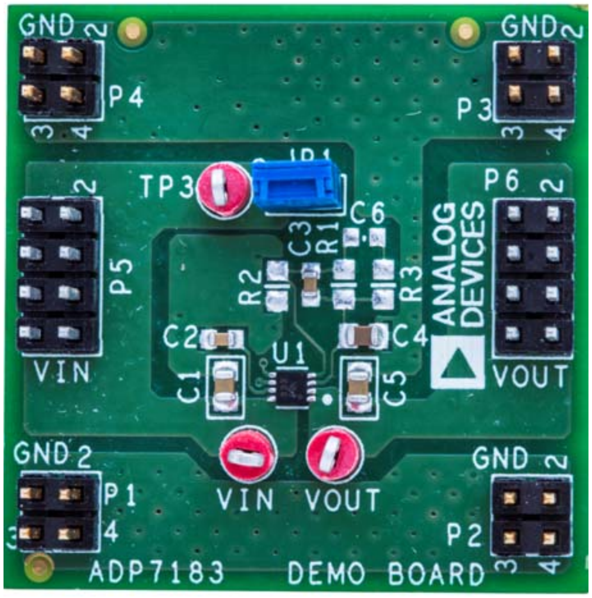


Figure 53. Evaluation Board

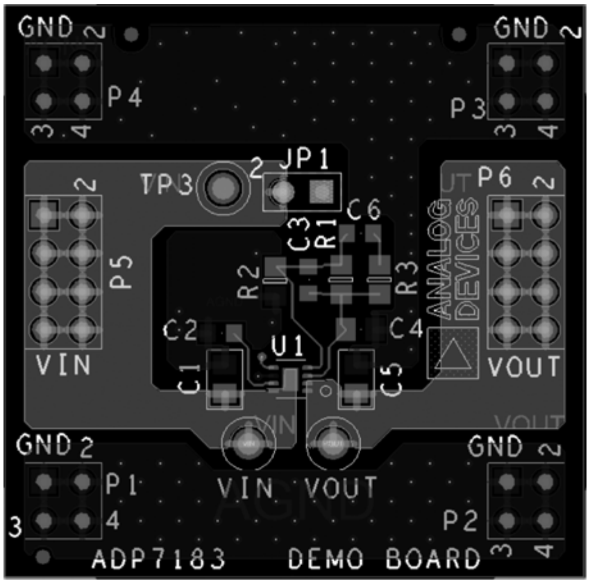


Figure 54. Typical Board Layout, Top Side

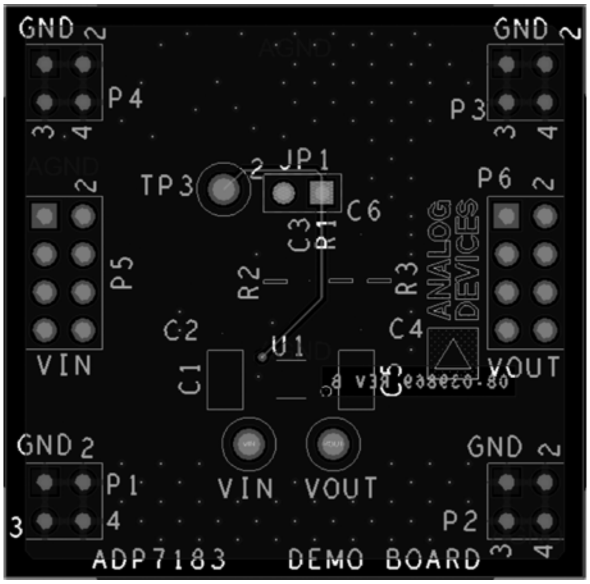
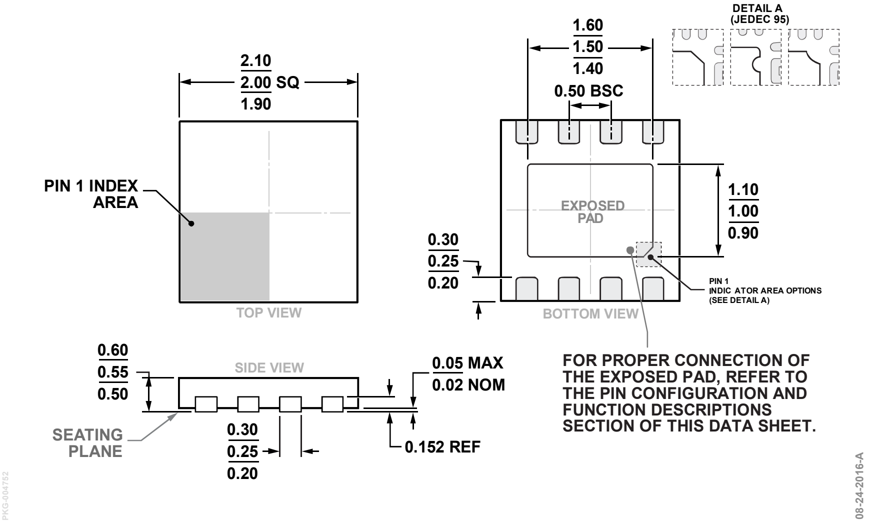


Figure 55. Typical Board Layout, Bottom Side

OUTLINE DIMENSIONS



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Figure 56. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.55 mm Package Height
(CP-8-27)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP7183ACPZN0.5-R7	−40°C to +125°C	−0.5	8-Lead LFCSP	CP-8-27	LS9
ADP7183ACPZN1.0-R7	−40°C to +125°C	−1.0	8-Lead LFCSP	CP-8-27	LSA
ADP7183ACPZN1.2-R7	−40°C to +125°C	−1.2	8-Lead LFCSP	CP-8-27	LSB
ADP7183ACPZN1.5-R7	−40°C to +125°C	−1.5	8-Lead LFCSP	CP-8-27	LSC
ADP7183ACPZN1.8-R7	−40°C to +125°C	−1.8	8-Lead LFCSP	CP-8-27	LSD
ADP7183ACPZN2.0-R7	−40°C to +125°C	−2.0	8-Lead LFCSP	CP-8-27	LSS
ADP7183ACPZN2.5-R7	−40°C to +125°C	−2.5	8-Lead LFCSP	CP-8-27	LSE
ADP7183ACPZN3.0-R7	−40°C to +125°C	−3.0	8-Lead LFCSP	CP-8-27	LSF
ADP7183ACPZN3.3-R7	−40°C to +125°C	−3.3	8-Lead LFCSP	CP-8-27	LTM
ADP7183ACPZN-R7	−40°C to +125°C	Adjustable	8-Lead LFCSP	CP-8-27	LS8
ADP7183-3.3-EVALZ		−3.3	Evaluation Board for the Fixed Voltage Option		
ADP7183-ADJ-EVALZ		−2.5	Evaluation Board for the Adjustable Voltage Option		

[1] Z = RoHS Compliant Part.

[2] For additional voltage options, contact a local Analog Devices Inc., sales or distribution representative.

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